

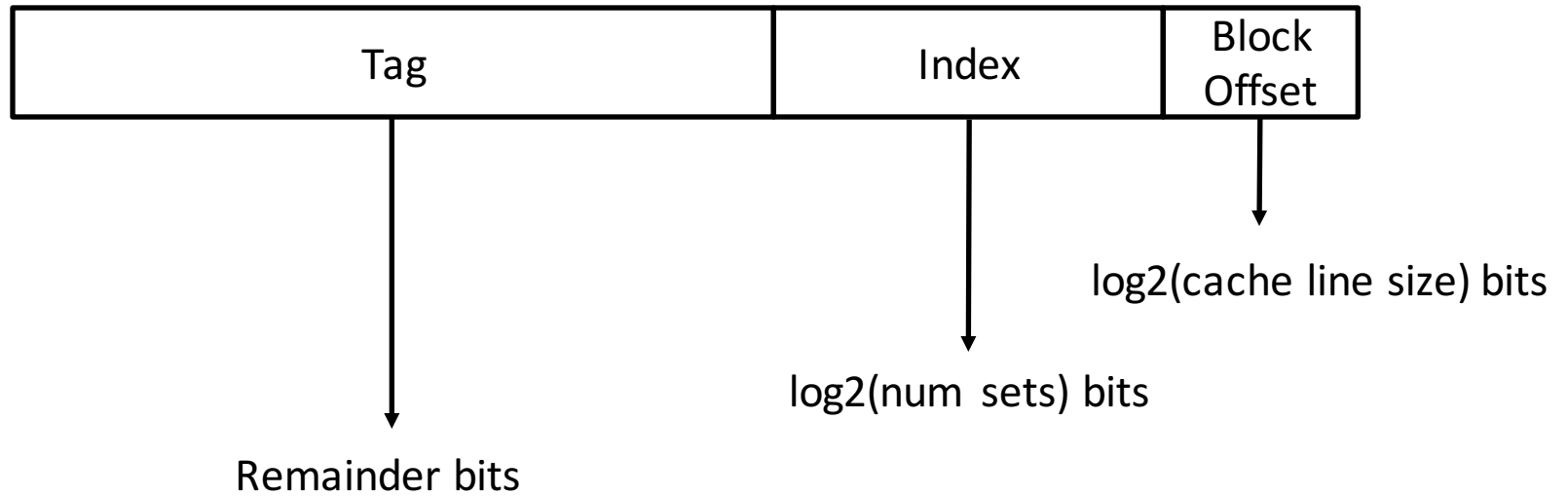
Quiz 1 Review

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EDSAC

- Accumulator based
- No concept Index Registers, PC
- Use self-modifying code for indirect accesses, subroutine calls etc.

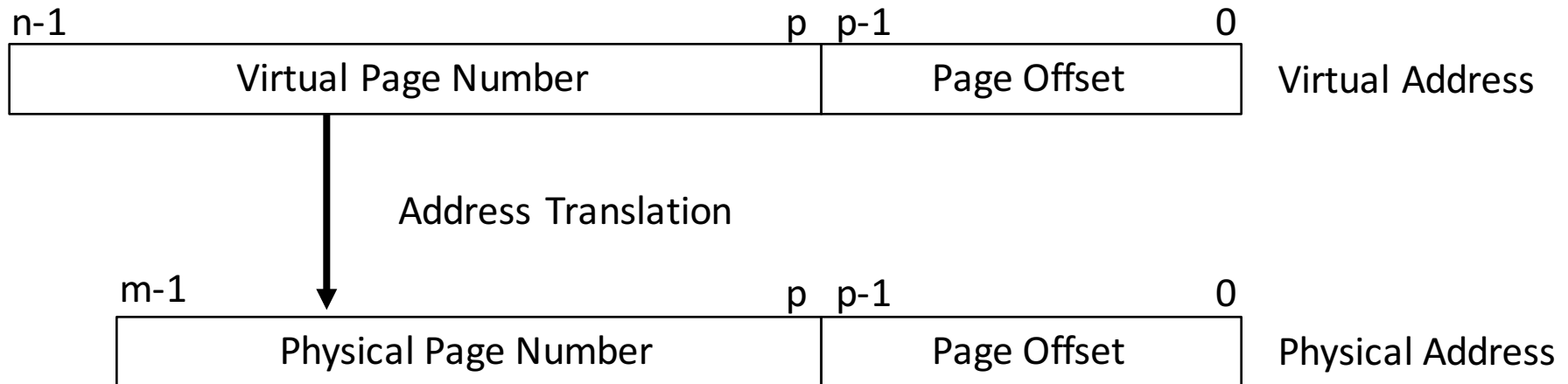
Caches



Address Translation

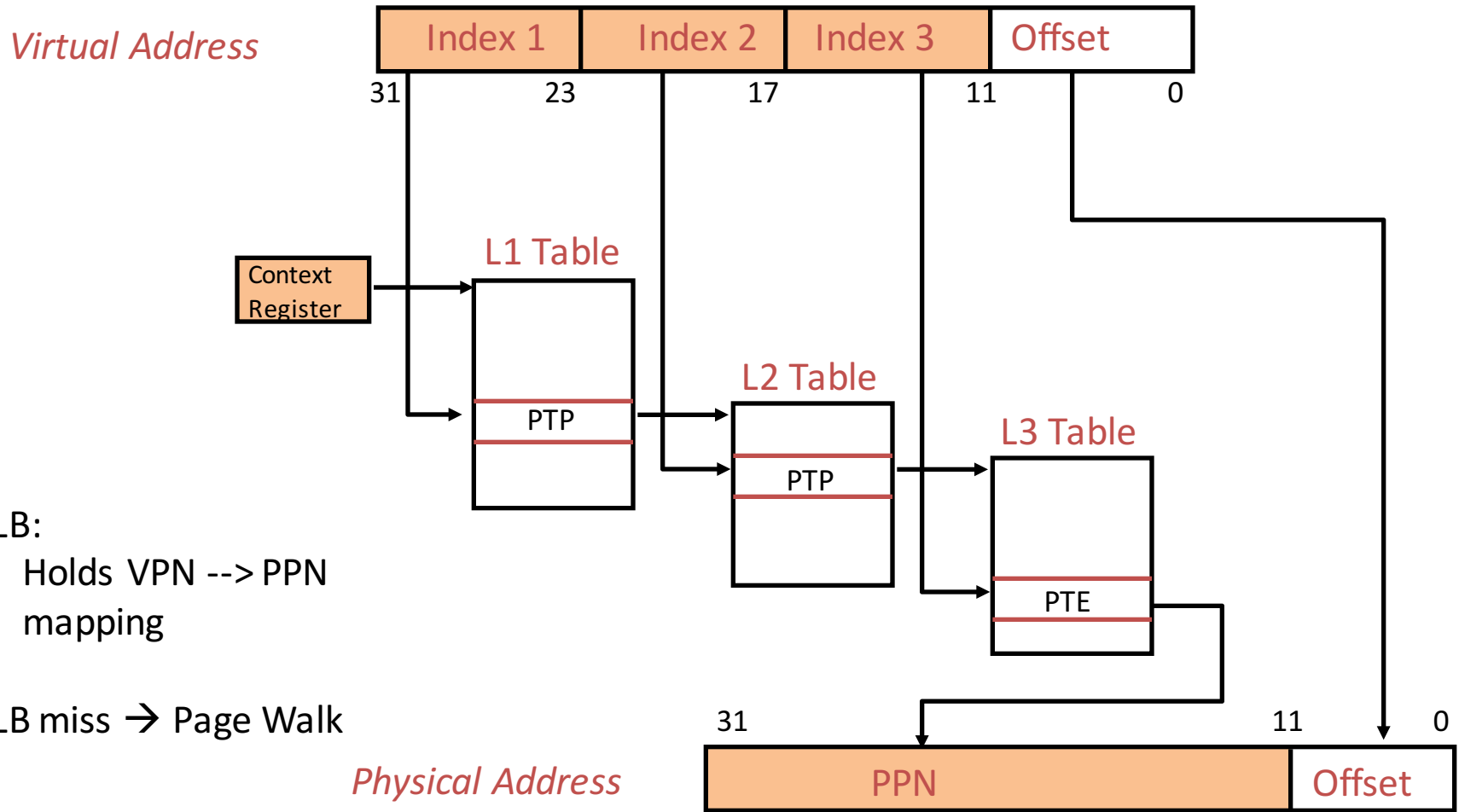
Parameters

- $P = 2^p =$ page size (bytes).
- $N = 2^n =$ Virtual-address limit
- $M = 2^m =$ Physical-address limit



Page offset bits do not change with translation

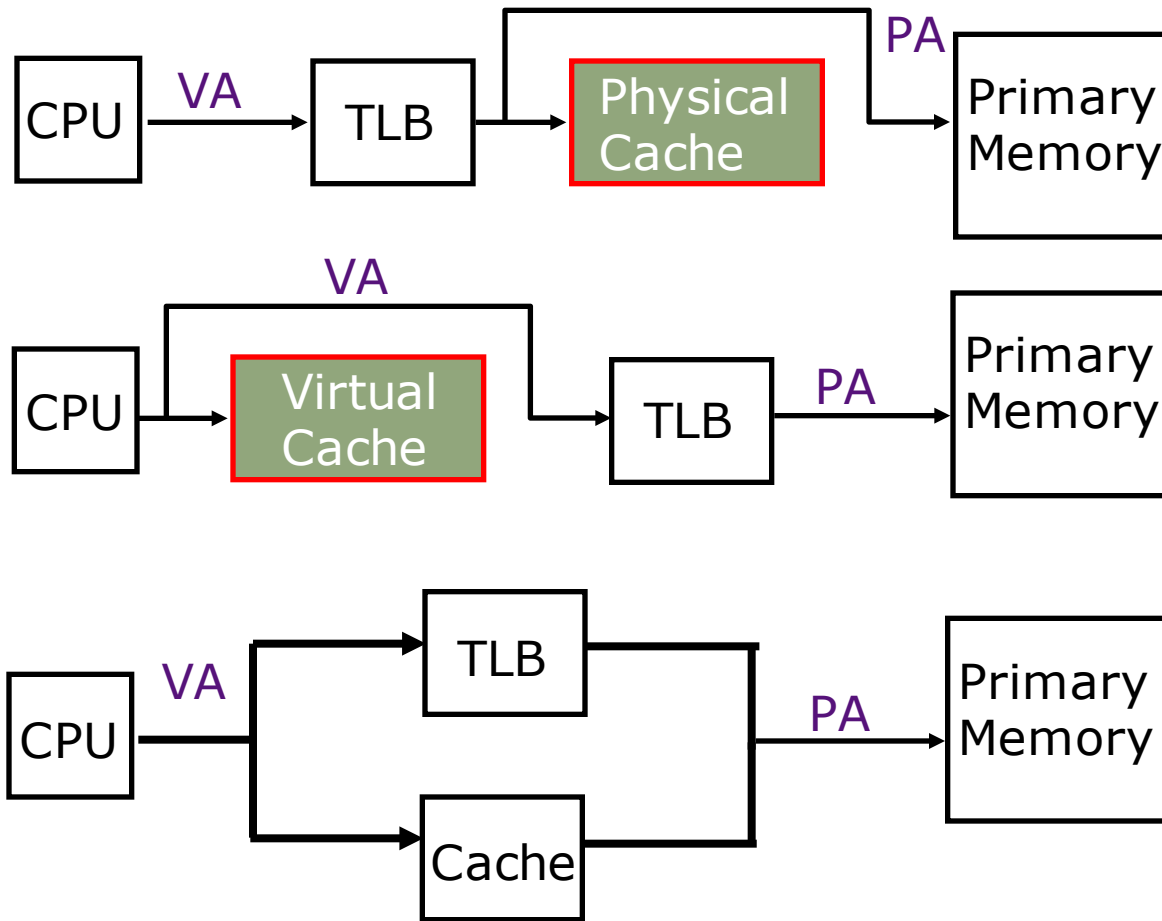
Hierarchical Page Tables



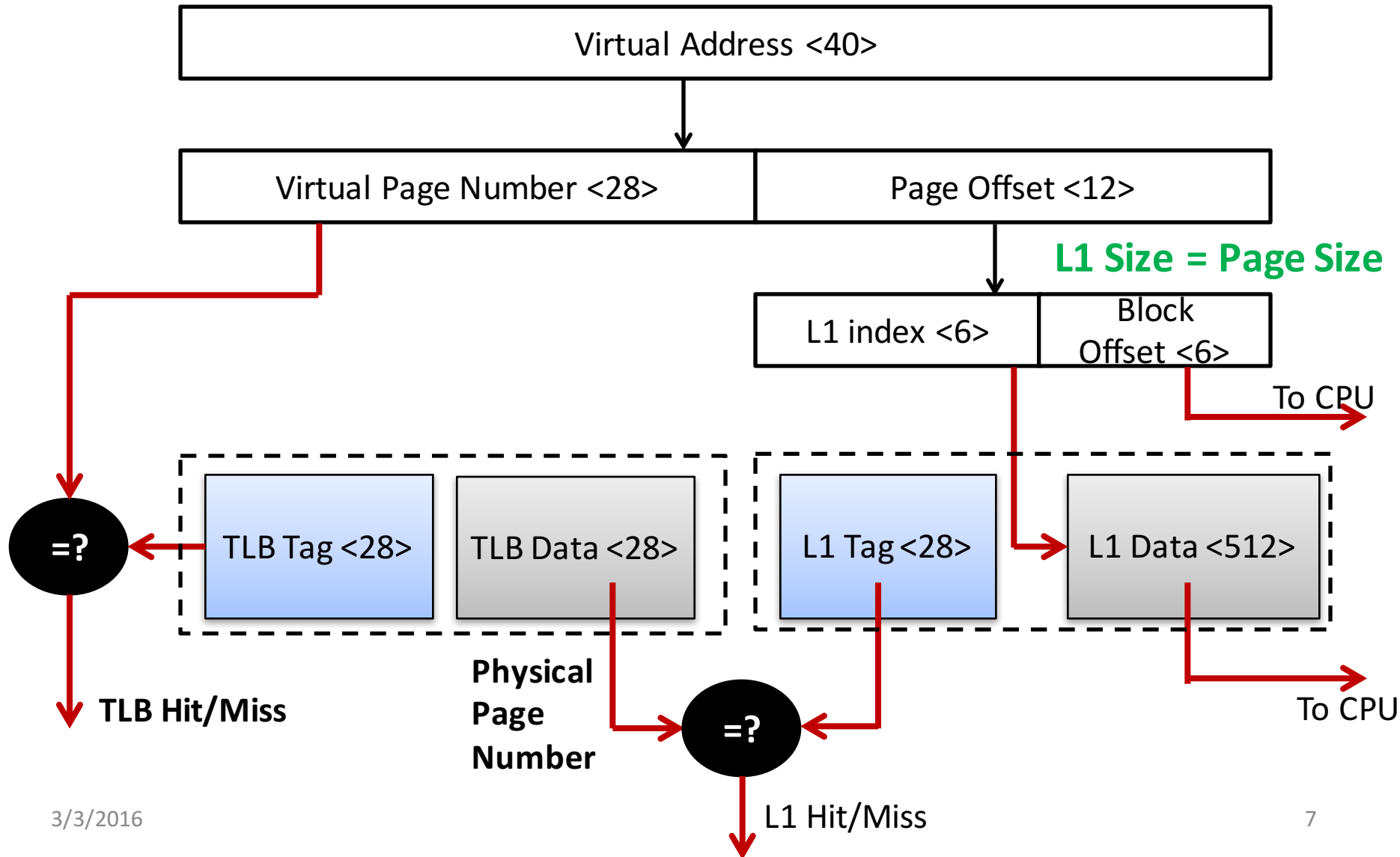
- TLB:
- Holds VPN --> PPN mapping

TLB miss → Page Walk

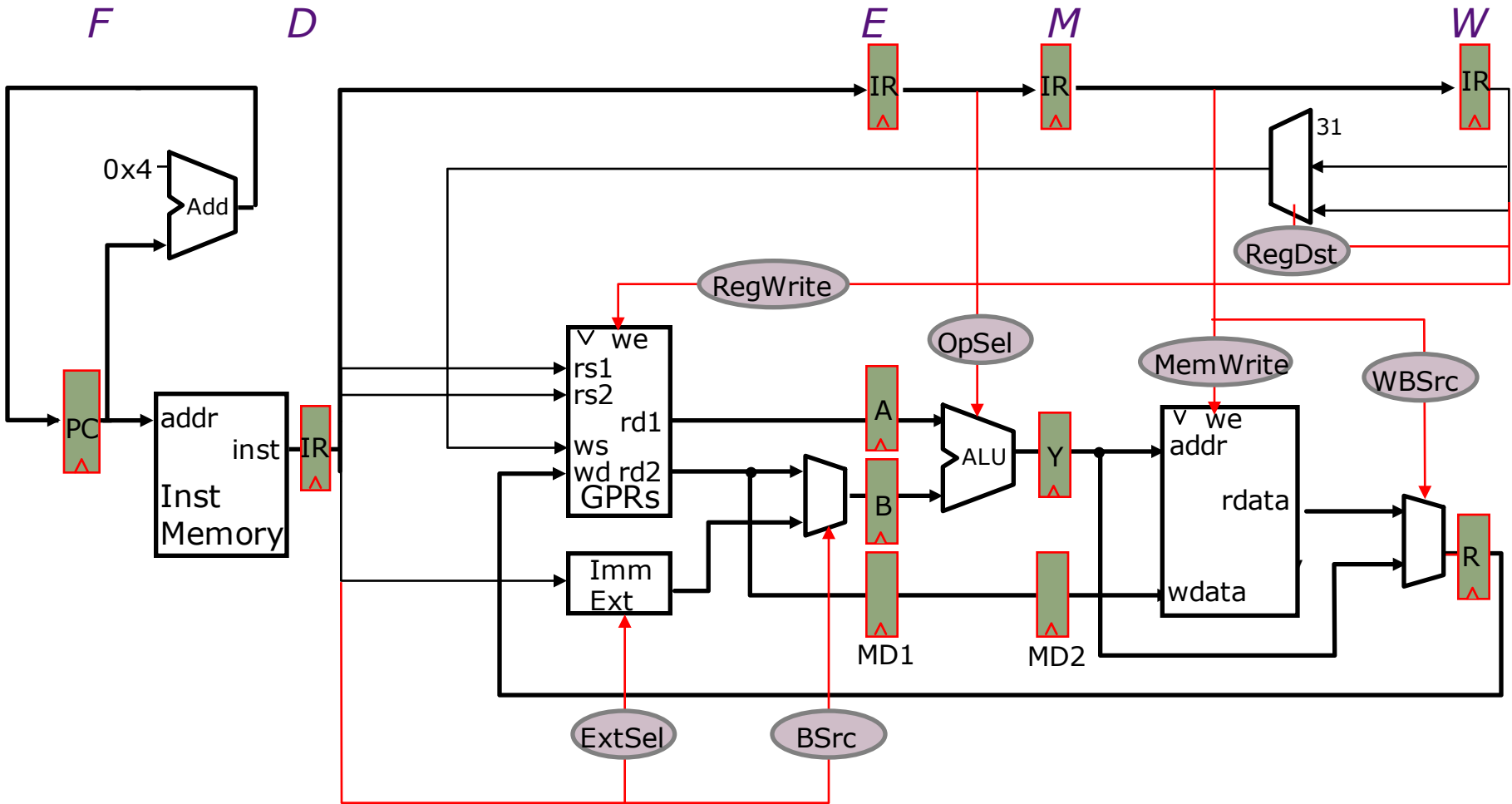
Physical vs Virtual Address Caches?



Concurrent Accesses to TLB and Cache



Pipelining



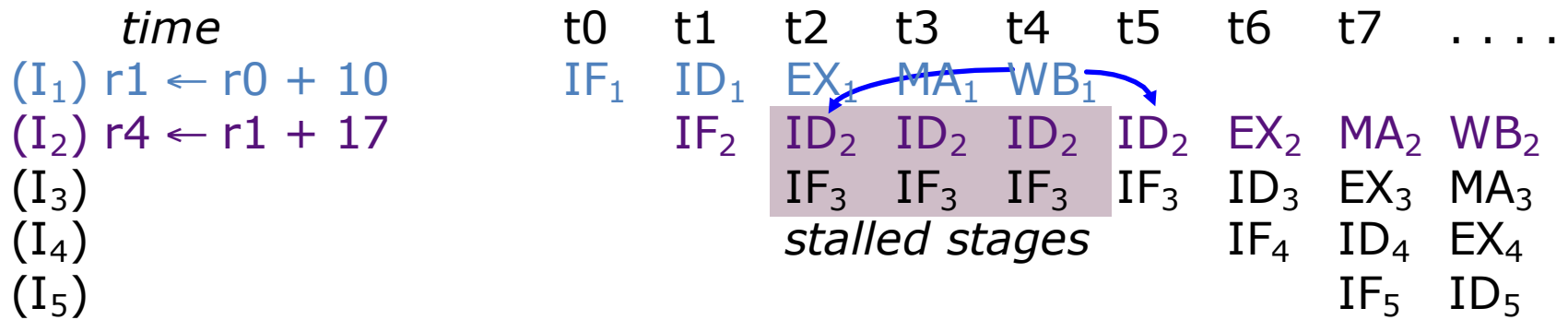
Pipeline Hazards

1. Structural
2. Data
3. Control

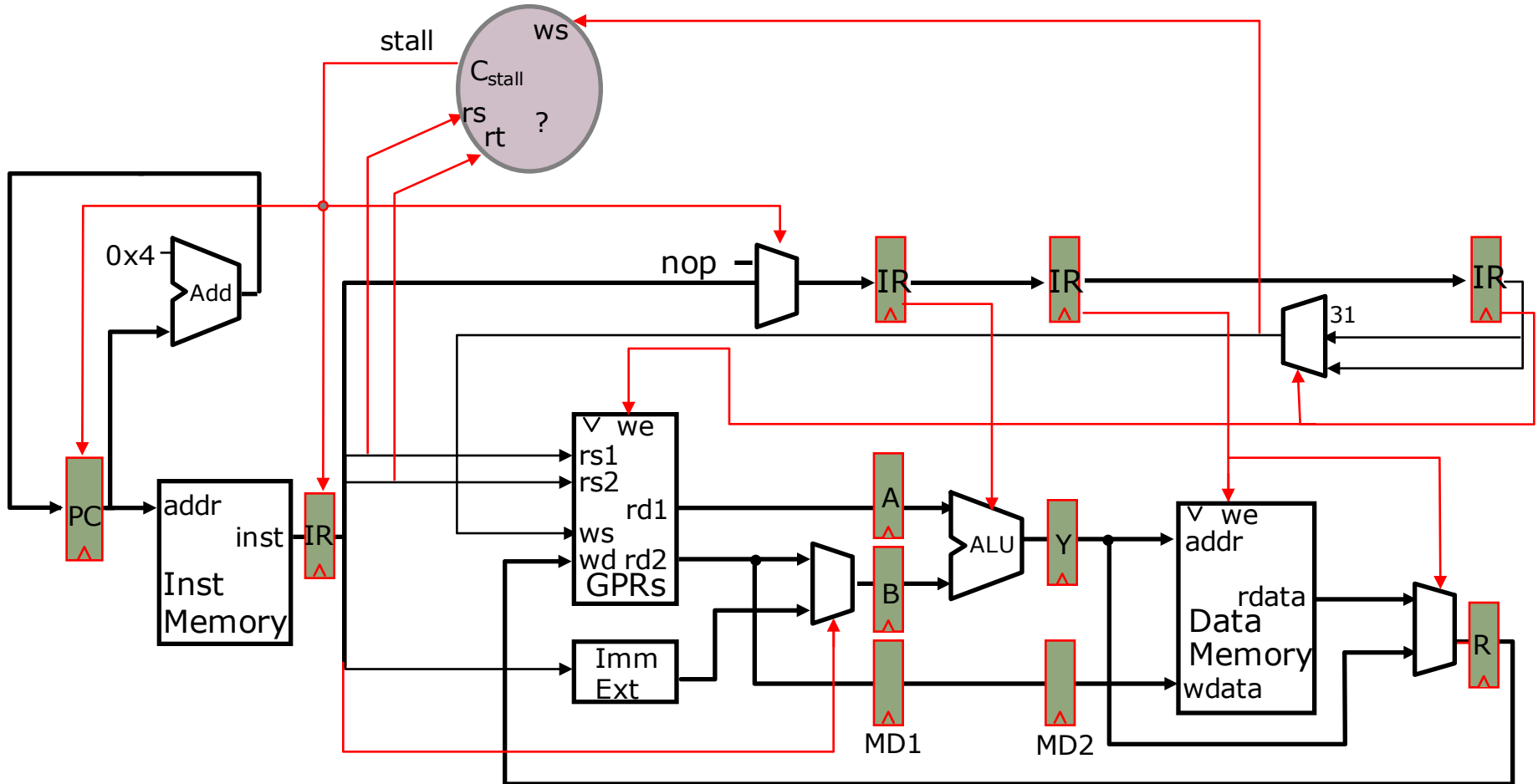
Handling Pipeline Hazards: Recipe

1. Stall
2. Bypass
3. Speculate

Instruction Flow Diagram



Pipelining



Compare the *source registers* of the instruction in the decode stage with the *destination register* of the *uncommitted instructions*.

Mechanics of Processor Design

- Analyze ISA
 - Determine data path requirements
- Select components of data path
 - ALU, Register file etc.
- Analyze implementation of instruction
 - Do we need to bypass, stall, speculate?
 - Assemble control signals

That's All!

Wish you all the best 😊